What is claimed is:

1. A method of acquisition a signal having a low signal to noise ratio (SNR), said method comprising the steps of:

(A) detecting a non-zero power in said signal having said low SNR during a power detect process;

(B) receiving said signal having said low SNR by using a signal receiver having an antenna;

(C) accumulating a plurality of digital samples of said signal within a predetermined period of time;

and

(D) employing an algorithm to correct defects in reception of said signal having said low SNR by minimizing a set of parameters selected from the group consisting of: {a carrier frequency offset; a code phase offset; and a data bit misalignment}.

2. The method of claim 1 further including the step of:

(E) performing tracking of said corrected received signal having said low SNR.

3. The method of claim 1, wherein said signal having said low SNR is emanating from a source selected from the group consisting of {a GPS satellite; a GLONASS satellite; a GALILEO satellite; and a pseudolite}, and wherein said step (C) of accumulating said plurality of digital samples of said signal further includes the step of a memory logging process further comprising the steps of:

(C1) employing an integer N plurality of In phase channel correlators configured to accumulate a plurality of I channel digital samples of said incoming signal in an In phase (I) channel, and employing said integer N plurality of Quadrature channel correlators configured to accumulate a plurality of Q channel digital samples of said incoming signal during a predetermined time period;

(C2) writing into a first memory block a plurality of I channel digital samples of said incoming signal accumulated during said predetermined time period, and writing into a second memory block s a plurality of Q channel digital samples of said incoming signal accumulated during said predetermined time period to complete a loop cycle of said memory logging process;

(C3) adjusting a code phase by using an expected code frequency offset deducted from a carrier frequency offset given by said power detect process to maintain a code phase of said incoming signal during said memory logging process;

(C4) counting a number of completed loop cycles;

(C5) if said number of completed loop cycles of said memory logging process is less than a predetermined integer number M of loop cycles, repeating said steps (C1-C5);

and

(C6) if a number of said completed loop cycles of said memory logging process is equal to said predetermined integer number M of loop cycles, ending said memory logging process.

4. The method of claim 1, wherein said step (D) of employing said algorithm to correct defects in reception of said signal having said low SNR further includes

the step of:

(D1) analyzing said stored digital samples of said signal accumulated within said predetermined period of time in order to determine said set of parameters selected from the group consisting of: {said carrier frequency offset; said code phase offset; and said data bit misalignment}; wherein an optimized acquisition of said signal having said low SNR corresponds to a set of minimized parameters selected from the group consisting of: {a minimized carrier frequency offset, a minimized code phase offset , and a minimized data bit misalignment}.

5. The method of claim 1, wherein said step (D) of employing said algorithm to correct defects in reception of said signal having said low SNR further includes the step of:

(D2) performing a carrier frequency false lock detection process to maximize the probability that said signal receiver is locked on a signal emanating from a signal source having a maximum signal power.

6. The method of claim 5, wherein said step (D2) of performing said carrier frequency false lock detection process further comprises the steps of:

(D2,1) selecting a starting carrier frequency;

(D2,2) computing a starting signal power at said starting carrier frequency;

(D2,3) selecting a subsequent carrier frequency;

(D2,4) computing a subsequent signal power at said subsequent carrier frequency;

(D2,5) comparing said subsequent signal power at said subsequent carrier frequency with a signal power at a preceding carrier frequency and selecting a

carrier frequency having the largest signal power;

and

(D2, 6) repeating said steps (D2,2) -(D2,5) until all carrier frequencies are processed.

7. The method of claim 1, wherein said step (D) of employing said algorithm to correct defects in reception of said signal having said low SNR further includes the step of:

(D3) performing an iterative optimization of a carrier frequency offset.

8. The method of claim 7, wherein said step (D3) of performing said iterative optimization of said carrier frequency offset further comprises the steps of:

(D3,1) selecting a carrier frequency offset from a set of data stored in said first memory and second memory;

(D3,2) reading an integer K plurality of stored I digital samples having a first carrier frequency from said first memory and reading said integer K plurality of stored Q digital samples having said first carrier frequency from said second memory by using a microprocessor;

(D3,3) performing a complex mix operation on said read values of said K plurality of stored I digital samples and said integer K plurality of stored Q digital samples having said first carrier frequency to generate a set of new values of said K plurality of I digital samples and said integer K plurality of Q digital samples having a second carrier frequency;

(D3,4) replacing in said first memory said integer K plurality of originally stored I digital samples having said first carrier frequency by said new values of

said integer K plurality of I digital samples having said second carrier frequency, and replacing in said second memory said integer K plurality of originally stored Q digital samples having said first carrier frequency by said new values of said integer K plurality of Q digital samples having said second carrier frequency;

and

(D3,5) repeating said steps (D3,2) -(D3,4) until all I digital samples in said first memory and all Q digital samples in said second memory are processed.

9. The method of claim 8, wherein said step (D3) of performing said iterative optimization of said carrier frequency offset further comprises the steps of:

(D3,6) selecting a carrier frequency offset from a set of data stored in said first memory and second memory;

(D3,7) reading an integer K plurality of stored I digital samples having a first carrier frequency from said first memory and reading said integer K plurality of stored Q digital samples having said first carrier frequency from said second memory by using a microprocessor;

(D3,8) performing a complex mix operation on said read values of said K plurality of stored I digital samples and said integer K plurality of stored Q digital samples having said first carrier frequency to generate a set of new values of said K plurality of I digital samples and said integer K plurality of Q digital samples having a second carrier frequency;

and

(D3,9) using said set of new values of said K plurality of I digital samples having said second carrier frequency and said integer K plurality of Q digital samples having said second carrier frequency for further processing.

10. The method of claim 1, wherein said step (D) of employing said algorithm to correct defects in reception of said signal having said low SNR further includes the steps of:

(D4) running a data transition algorithm to minimize said data bit misalignment parameter;

(D5) running a carrier frequency estimation algorithm to minimize said carrier frequency offset parameter;

(D6) running a code phase estimation algorithm to minimize said code phase offset;

and

(D7) repeating said steps (D4-D6) until each said parameter selected from the group consisting of: {said carrier frequency offset; said code phase offset; and said data bit misalignment} converges on a corresponding minimized parameter selected from the group consisting of: {said minimized carrier frequency offset; said minimized code phase offset; and said minimized data bit misalignment}.

11. The method of claim 10, wherein said step (D4) of running said data transition algorithm to minimize said data bit misalignment parameter further comprises the steps of:

(D4,1) determining the power of the difference between adjacent correlations taken over the entire correlator data set stored in said first memory and stored in said second memory;

and

(D4,2) summing said power of the difference between said adjacent

correlations determined in said step (D4,1) over all possible data bit positions;

wherein said data transition algorithm cancels or enhances said received signal based on a presence or on absence of a data bit transition.

12. The method of claim 10, wherein said step (D5) of running said carrier frequency estimation algorithm to minimize said carrier frequency offset parameter further comprises the steps of:

(D5,1) accumulating the I and Q memory samples across a bit time period;

(D5,2) selecting the I and Q memory samples closest to a correlation peak;

(D5,3) estimating the phase of the carrier signal using said I and Q memory samples closest to said correlation peak;

(D5,4) estimating the frequency of the carrier signal by using difference sequential carrier measurements;

(D5,5) averaging said carrier frequency estimates across the entire data stored in said fist and second memory;

and

(D5,6) using the resulting averaged frequency offset value for subsequent data processing.

13. The method of claim 10, wherein said step (D6) of running said code phase estimation algorithm to minimize said code phase offset further comprises the steps of:

(D6,1) accumulating an Early, Punctual, and Late correlator values over said predetermined memory logging time period in both I and Q channels;

(D6,2) computing a correlation vector magnitude for each said Early,

Punctual, and Late accumulated correlator values for each said bit period;

(D6,3) summing said correlation vector magnitude for each said Early, Punctual, and Late correlators over said predetermined memory logging time period to compute a peak equation; wherein said peak equation represents an optimized direction and an optimized size of a code phase error;

(D6,4) using said peak equation to compute a code phase error;

and

(D6,5) using said code phase error to achieve an optimized code tracking function.

14. The method of claim 2, wherein said step (E) of performing tracking of said corrected received signal having said low SNR further includes the steps of:

(E1) loading said first memory block and said second memory block with a set of current I and Q digital samples of said received signal collected during said predetermined time period;

(E2) running said data transition algorithm to minimize said data bit misalignment parameter; running said carrier frequency estimation algorithm to minimize said carrier frequency offset parameter; and running said code phase estimation algorithm to minimize said code phase offset thus correcting said received signal having said low SNR;

(E3) performing a tracking function of said received corrected signal having said low SNR by applying said minimized carrier frequency offset and applying said minimized code phase offset to a Digital Signal Processing (DSP) block;

and

(E4) repeating said steps ((E1)- (E3)) until said tracking of said received corrected signal having said low SNR is continued.

15. The method of claim 15, wherein said step (E3) of performing said tracking function of said received corrected signal having said low SNR further includes the steps of:

(E3,1) closing a code tracking loop;

(E3,2) closing a carrier tracking loop;

(E3,3) aligning data bit edges;

and

(E3,4) performing a data extraction operation and performing a pseudo range measurement operation by using said received corrected signal having said low SNR.

16. A method of running a data transition algorithm to minimize a data bit misalignment parameter for a received signal having a low SNR, said method comprising the steps of:

(F1) determining the power of the difference between adjacent correlations taken over an I correlator data set stored in a first memory and taken over a Q correlator data set stored in a second memory;

and

(F2) summing said power of the difference between said adjacent correlations determined in said step (F1) over all possible data bit positions;

wherein said data transition algorithm cancels or enhances said received signal based on a presence or on absence of a data bit transition.

17. A method of running a carrier frequency estimation algorithm to minimize a carrier frequency offset parameter for a received signal having a low SNR, said method comprising the steps of:

(G1) accumulating the I and Q memory samples across a bit time period;

(G2) selecting the I and Q memory samples closest to a correlation peak;

(G3) estimating the phase of the carrier signal using said I and Q memory samples closest to said correlation peak;

(G4) estimating the frequency of the carrier signal by using difference sequential carrier measurements;

(G5) averaging said carrier frequency estimates across the entire data stored in said fist and second memory;

and

(G6) using the resulting averaged frequency offset value for subsequent data processing.

18. A method of running a code phase estimation algorithm to minimize a code phase offset for a received signal having a low SNR, said method comprising the steps of:

(H1) accumulating an Early, Punctual, and Late correlator values over said predetermined memory logging time period in both I and Q channels;

(H2) computing a correlation vector magnitude for each said Early, Punctual, and Late accumulated correlator values for each said bit period;

(H3) summing said correlation vector magnitude for each said Early, Punctual, and Late correlators over said predetermined memory logging time period to compute a peak equation; wherein said peak equation represents an

optimized direction and an optimized size of a code phase error;

(H4) using said peak equation to compute a code phase error;

and

(H5) using said code phase error to achieve an optimized code tracking function.

19. A computer-readable storage medium useful in association with a Digital Signal Processor (DSP) chip; said DSP chip having a processor and memory, said computer- readable storage medium including computer-readable code instructions configured to cause said processor to execute the steps of:

(F1) determining the power of the difference between adjacent correlations taken over an I correlator data set stored in a first memory and taken over a Q correlator data set stored in a second memory for a received signal having a low SNR;

and

(F2) summing said power of the difference between said adjacent correlations determined in said step (F1) over all possible data bit positions;

wherein said received signal is canceled or enhanced based on a presence or on absence of a data bit transition.

20. A computer-readable storage medium useful in association with a Digital Signal Processor (DSP) chip; said DSP chip having a processor and memory, said computer- readable storage medium including computer-readable code instructions configured to cause said processor to execute the steps of:

(G1) accumulating the I and Q memory samples across a bit time period for a received signal having a low SNR;

(G2) selecting the I and Q memory samples closest to a correlation peak;

(G3) estimating the phase of the carrier signal using said I and Q memory samples closest to said correlation peak;

(G4) estimating the frequency of the carrier signal by using difference sequential carrier measurements;

(G5) averaging said carrier frequency estimates across the entire data stored in said fist and second memory;

and

(G6) using the resulting averaged frequency offset value for subsequent data processing.

21. A computer-readable storage medium useful in association with a Digital Signal Processor (DSP) chip; said DSP chip having a processor and memory, said computer- readable storage medium including computer-readable code instructions configured to cause said processor to execute the steps of:

(H1) accumulating an Early, Punctual, and Late correlator values over said predetermined memory logging time period in both I and Q channels for a received signal having a low SNR;

(H2) computing a correlation vector magnitude for each said Early, Punctual, and Late accumulated correlator values for each said bit period;

(H3) summing said correlation vector magnitude for each said Early, Punctual, and Late correlators over said predetermined memory logging time

period to compute a peak equation; wherein said peak equation represents an optimized direction and an optimized size of a code phase error;

(H4) using said peak equation to compute a code phase error;

and

(H5) using said code phase error to achieve an optimized code tracking function.

22. A computer program product that includes a computer-readable medium having a sequence of instructions which, when executed by a processor, causes the processor to execute a process for optimizing a reception of a signal having a low SNR, the process comprising:

(F1) determining the power of the difference between adjacent correlations taken over an I correlator data set stored in a first memory and taken over a Q correlator data set stored in a second memory for a received signal having a low SNR;

and

(F2) summing said power of the difference between said adjacent correlations determined in said step (F1) over all possible data bit positions;

wherein said received signal is canceled or enhanced based on a presence or on absence of a data bit transition.

23. A computer program product that includes a computer-readable medium having a sequence of instructions which, when executed by a processor, causes the processor to execute a process for optimizing a reception of a signal having a low SNR, the process comprising:

(G1) accumulating the I and Q memory samples across a bit time period for a received signal having a low SNR;

(G2) selecting the I and Q memory samples closest to a correlation peak;

(G3) estimating the phase of the carrier signal using said I and Q memory samples closest to said correlation peak;

(G4) estimating the frequency of the carrier signal by using difference sequential carrier measurements;

(G5) averaging said carrier frequency estimates across the entire data stored in said fist and second memory;

and

(G6) using the resulting averaged frequency offset value for subsequent data processing.

24. A computer program product that includes a computer-readable medium having a sequence of instructions which, when executed by a processor, causes the processor to execute a process for optimizing a reception of a signal having a low SNR, the process comprising:

(H1) accumulating an Early, Punctual, and Late correlator values over said predetermined memory logging time period in both I and Q channels for a received signal having a low SNR;

(H2) computing a correlation vector magnitude for each said Early, Punctual, and Late accumulated correlator values for each said bit period;

(H3) summing said correlation vector magnitude for each said Early, Punctual, and Late correlators over said predetermined memory logging time period to compute a peak equation; wherein said peak equation represents an

optimized direction and an optimized size of a code phase error;

(H4) using said peak equation to compute a code phase error;

and

(H5) using said code phase error to achieve an optimized code tracking function.

25. An apparatus for acquisition of a signal having a low signal to noise ratio (SNR), said apparatus comprising:

(A) a means for detecting a non-zero power in said signal having said low SNR during a power detect process;

(B) a means for receiving said signal having said low SNR;

(C) a means for accumulating a plurality of digital samples of said signal within a predetermined period of time;

(D) a means for correcting defects in reception of said signal having said low SNR by minimizing a set of parameters selected from the group consisting of: {a carrier frequency offset; a code phase offset; and a data bit misalignment};

and

(E) a means for tracking said corrected received signal having said low SNR.

26. The apparatus of claim 25, wherein said means (C) for accumulating said plurality of digital samples of said signal further includes:

(C1) an integer N plurality of In phase channel correlators configured to accumulate an integer N plurality of digital samples of said incoming signal in an In phase (I) channel, and said integer N plurality of Quadrature channel

correlators configured to accumulate a first plurality of digital samples of said incoming signal during a predetermined time period;

(C2) a first memory block configured to store a plurality of I channel digital samples of said incoming signal accumulated during said predetermined time period, and a second memory block configured to store a plurality of Q channel digital samples of said incoming signal accumulated during said predetermined time period;

and

(C3) a counter configured to count a number of complete loop cycles.

27. The apparatus of claim 25, wherein said means (D) for correcting said defects in reception of said signal having said low SNR further includes an algorithm comprising at least the following steps:

(D1) selecting a starting carrier frequency;

(D2) computing a starting signal power at said starting carrier frequency;

(D3) selecting a subsequent carrier frequency;

(D4) computing a subsequent signal power at said subsequent carrier frequency;

(D5) comparing said subsequent signal power at said subsequent carrier frequency with a signal power at a preceding carrier frequency and selecting a carrier frequency having the largest signal power;

and

(D6) repeating said steps (D2) -(D5) until all carrier frequencies are processed.

28. The apparatus of claim 25, wherein said means (D) for correcting said defects in reception of said signal having said low SNR further includes an algorithm comprising at least the following steps:

(D7) selecting a carrier frequency offset from a set of data stored in said first memory and second memory;

(D8) reading an integer K plurality of stored I digital samples having a first carrier frequency from said first memory and reading said integer K plurality of stored Q digital samples having said first carrier frequency from said second memory by using a microprocessor;

(D9) performing a complex mix operation on said read values of said K plurality of stored I digital samples and said integer K plurality of stored Q digital samples having said first carrier frequency to generate a set of new values of said K plurality of I digital samples and said integer K plurality of Q digital samples having a second carrier frequency;

and

(D10) using said set of new values of said K plurality of I digital samples having said second carrier frequency and said integer K plurality of Q digital samples having said second carrier frequency for further processing.

29. The apparatus of claim 25, wherein said means (D) for correcting said defects in reception of said signal having said low SNR further includes an algorithm comprising at least the following steps:

(D11) running a data transition algorithm to minimize said data bit misalignment parameter;

(D12) running a carrier frequency estimation algorithm to minimize said

carrier frequency offset parameter;

(D13) running a code phase estimation algorithm to minimize said code phase offset;

and

(D14) repeating said steps (D11-D13) until each said parameter selected from the group consisting of: {said carrier frequency offset; said code phase offset; and said data bit misalignment} converges on a corresponding minimized parameter selected from the group consisting of: {said minimized carrier frequency offset; said minimized code phase offset; and said minimized data bit misalignment}.

30. The apparatus of claim 25, wherein said (E) means for tracking said corrected received signal having said low SNR further includes:

(E1) a means for applying said minimized carrier frequency offset and for applying said minimized code phase offset to a Digital Signal Processing (DSP) block.

31. The apparatus of claim 30, wherein said means for applying said minimized carrier frequency offset and for applying said minimized code phase offset to a Digital Signal Processing (DSP) block further includes:

a code tracking loop;

a carrier tracking loop;

a means for aligning data bit edges; and

a means for data extraction from said received corrected signal having said low SNR.